ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device including a memory cell array in which nonvolatile semiconductor memory devices (memory cells) are arranged in a matrix with a plurality of rows and columns. The nonvolatile semiconductor memory device includes a word gate formed on a semiconductor substrate with a first gate insulating layer interposed, an impurity diffusion layer formed in the semiconductor substrate which forms either a source region or a drain region, and first and second control gates in the shape of sidewalls formed along either side of the word gate. Each of the first and second control gates is disposed on the semiconductor substrate with a second gate insulating layer interposed, and also on the word gate with a side insulating layer interposed. The first and second control gates extend in the column direction. A pair of first and second control gates which are adjacent in the row direction is connected to a common contact section.